Software package for optimizing digital circuits

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Window approach

- We extract a combinational fragment of a large digital circuit for optimization.
- For optimizing the fragment we divide it into two parts which are optimized independently.
Optimizing a head component of a combinational circuit

The behaviour of a combinational circuit is described by three behavioral functions $\Psi_f$, $\Psi_g$, $\Psi_h$.

The largest solution can be found as $\left(\Psi_g \land \Psi_h\right)_{x, u}$.
Can we select a function equal to 0?

- Derive a new function $\varphi$:
  $\varphi(x_1, x_2, \ldots, x_n, u_1, u_2, \ldots, u_k) = 1 \iff u_j = 0$
  ($\varphi = \neg u_j$)

- Derive the conjunction $\varphi \land (\Psi_g \land \Psi_h)_{x,u}$
  The function $u_j$ can be selected equal to 0 iff the formula
  $$\neg \left( \left( \varphi \land (\Psi_g \land \Psi_h)_{x,u} \right) \downarrow x \right)$$

is UNSAT
Can we select a function as a function of two input variables?

- Let $p(x_i, x_j)$ be a function of 2 input variables $x_i$ and $x_j$

- Add a new variable $u_{k+1} = u_s \oplus p(x_i, x_j)$

- The function $u_s$ can be represented as $u_s = p(x_i, x_j)$ iff the function $u_{k+1}$ can be selected as 0
Optimizing the tail component of a combinational circuit

- Represent the behavioural function of the tail component as DNF

- The function $y_k$ can be represented as $u_i \vee u_j$ iff the column corresponding to $y_k$ is the disjunction of the columns corresponding to $u_i$ and $u_j$
Data representation

- All names are hashed by integer numbers
- Sequential circuit is represented as an array of its nodes
- Behavioural functions are represented as BDD using CUdd package
Main methods of package

- Window extraction and head-tail splitment
- Largest solution derivation for head and tail components
- Optimization (using, for head optimization, MiniSAT included into ABC)
- Replacement the window subcircuit with optimized one
Experimental results for the combinational circuits

- An average path length of an extracted fragment was 10 gates.
- Around 15% of benchmarks were optimized (the most significant were s298, s838, s420 circuits).
- When resynthesised with ABC the number of gates and the average length from primary inputs to outputs could be reduced in all circuits.
Current work

- Improving the software implementations to deal with larger benchmarks

- Working on algorithms and software implementations for sequential fragments
Thank you for your attention!