

Optimization of electronics component placement design on PCB using genetic algorithm

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Abstract—This article presents modified genetic algorithm (GA) of the placement of electronic components (EC) on a printed circuit board (PCB) considering criterias of thermal conditions and minimum weighted sum.

Keywords— *electronics component; printed circuit board; genetic algorithm; guillotine cutting; electronic device.*

I. INTRODUCTION

The trend of most electronic companies is towards designing more functionality but smaller packages electronic system. Therefore, solving these problems requires using a large number of criteria and constraints with high dimension initial data.

The objective is to reduce the time, increase quality and lower the cost of design for the design of PCB using CAD systems. The best results of PCB designer was achieved by such companies as Altium Designer, Mentor Graphics, National Instruments, Zuken. These companies develop packages for designing PCB, which have some advantages: large elements libraries, conversion of the files, inerrability of them in other CAD-systems, comfortable interface and etc. However, these systems have several disadvantages: the tasks consist only one criteria, ignore criteria of thermal conditions, in several systems there is also no automated placement of the EC on PCB. In this regard, there is a need to improve math and CAD software. The novelty of this work is to use the algorithm, for solving multi-criteria problem for placement EC on PCB.

II. PROBLEM STATEMENT

A. The purpose of the work

The purpose of the work is the development of a modified genetic algorithm of electronics component placement on a PCB, considering criteria of thermal conditions and minimum weighted sum.

B. Problem statement

Statement of the placement problem is to find the location coordinates of EC placement on PCB with the predefined criteria and constraints.

III. CRITERIA AND COONDITIONS FOR LOCATION PROBLEM

A criterion of thermal conditions is proposed for placement of elements. Fitness function for this criteria can be expressed as:

$$f_t = \sum_{i=1}^N \left| \sum_{\substack{j=1 \\ j \neq i}}^N (P_i - P_j) d_{ij} \right| \rightarrow \min \quad (1)$$

where N is number of EC located on PCB; P_i and P_j are the thermal power dissipation i and j EC; d_{ij} - distance between i and j EC.

Using this criterion allows evenly distributing the EC on PCB, which allows improving the quality of PCB.

Furthermore, it is proposed to take into account the criteria of minimum weighted sum. Fitness function for this criteria can be expressed as:

$$f_c = \sum_{i=1}^n \sum_{j=0}^n c_{ij} d_{ij} \rightarrow \min \quad (2)$$

where c_{ij} – number of links between i and j EC.

Using this criterion allows reducing the distance between the maximal connected EC, which simplifies the subsequent tracing and improves the electrical characteristics of the device.

III. GENETIC ALGORITHM FOR PLACEMENT EC ON PCB

A. Genetic algorithm

GA – is a search heuristic that mimics the process of natural evolution.

Key terms for using GA:

- Individual is one potential solution.
- Population is a set of potential solutions.
- Chromosome is code representation of solutions. Gen is cell chromosomes, which can change its value.
- Allele is numeric value of gene.
- Locus is location of a gene in chromosome.
- Fitness function
- Generation - one cycle of the GA, including a procedure for breeding, mutation breeding [3].

B. Genetic algorithm for placement EC on PCB

Genetic algorithm using of the guillotine cutting of material. The plan of cutting is carried a binary tree.

The algorithm of placement EC on PCB using GA include next steps:

Step 0. Input of initial data.

Initial data of the problem are:

1. The number of the EC.
2. The number of links between *i* and *j* EC.
3. The thermal power dissipation *i* and *j* EC.
4. The number of individuals in a population.
5. The number of generations of evolution.

Step 1. Creation of a new population. While creation of initial population a number individuals set at random. Each gene of chromosome gets its unique value.

Each solution is encoded by two chromosomes: XP1, XP2.

In contracts to the encoding of chromosomes proposed in articles [5], [6], we suggest another method of encoding chromosome XP1.

Chromosome XP1 contains coded information about the laying of the tree leaves, which indicate the order of the placement of EC on PCB: $XP1 = \{g_{li} \mid i = 1, 2, \dots, n\}$. Each gene g_{li} can take any value in the range $[1; n]$.

For example, $n=9$, XP1 (Fig.1): $\langle 4,2,1,3,5,9,6,7,8 \rangle$.

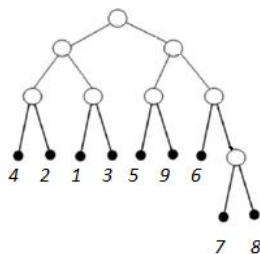


Fig.1. Binary tree for chromosome XP1

The proposed modification of the algorithm can significantly reduce the calculating time to solve the problem.

Chromosome XP2 contains coded information about the type of cut of PCB space.

Chromosome $XP2 = \{g_{2i} \mid i = 1, 2, \dots, n\}$ is the type of the cut (H or V).

The number of the gene XP2 is $n^* = n - 1$.

The gene value is 0 or 1, with 0 – V – vertical cutting, and 1 – H – horizontal cutting.

For example:

Lets, $n=9$, $XP2 = \langle 0, 1, 0, 0, 1, 1, 0, 1 \rangle$ (Fig. 2).

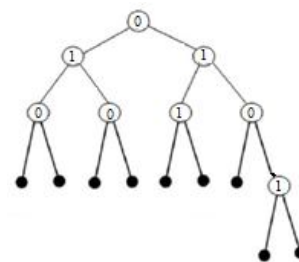


Fig. 2. Binary tree for chromosome XP2

Step 2. Crossover. All individuals of the population are formed in pairs at random. As soon as 2 solution-parents are selected, they are applied to a single-point crossover, which create two new solutions-offspring on their bases. Randomly selects one of the possible break point (Break point is the area between the adjacent bits in the string). Both parental structure are torn into two segments at this point. Then, segments of different parents stick together and produce two offsprings (Fig.3).

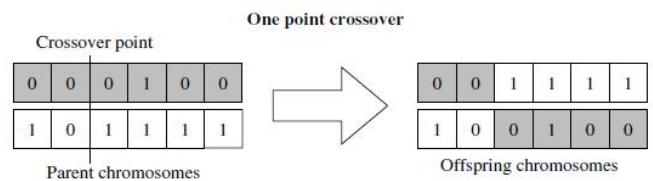


Fig.3. One point crossover

Step 3. Mutation. In case of mutations chromosomes undergoes some accidental modifications. In this work we propose using one-point mutation, where one bit in chromosome selects randomly and changes its value to the opposite one (Fig.4).

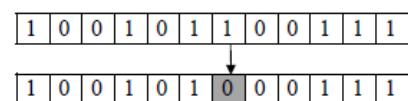


Fig.4. One-point mutation

Step 4. Designer of a binary tree cuts. Knowing the number EC, we can design the binary tree.

The total amount of EC (E_i) – is the top of parent (V_0). If E_i is not equal 2 or 3, E_i will divide by 2. The obtained values are rounded: the first figure in the smallest way, the second figure in the biggest way. The obtained tops (second level) are daughter vertex for V_0 . The first figure will be the first daughter vertex V_1 for V_0 , the second figure will be the second daughter vertex V_2 for V_0 .

If the value of obtained daughter vertex V_1 and V_2 is not equal 2 or 3, they are the top – parents, and they again might be halved. Halving will continue until all of the number of top-parents will be equal to two or three. With each subsequent level, the number of vertices will increase by 2^k , where k – level (Fig.5).

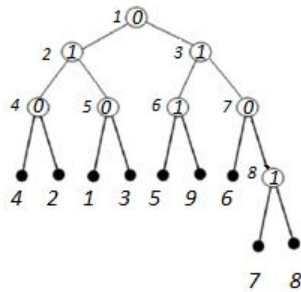


Fig.5. Binary tree cuts

When the number of top-parents is equal to 2, then top-parent correspond to the two binary tree leaves (Fig.6).



Fig.6. The example of the design binary tree cut

When number of top-parents is equal to 3, then top-parent corresponds to another top-parent, which owns two of the leaves and another binary tree leaf (Fig.7).

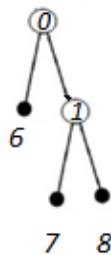


Fig.7. The example of the design of binary tree cut

Step 5. Binary convolution method. On the basis of this information, binary tree designer is carried out by means of serial binary convolution areas on the tree incisions, starting with tree leaves. Each inner top of binary tree corresponds the area, obtained in the result of the binary convolution of a subtree, with the root of the inner top. Consider that cut with number i is cutting the top d_i (area is u_i). In the beginning of convolution each top d_i , which is the leaf of the tree, is corresponding the area s_i with dimension $x_i = a_i$, $y_i = b_i$, that is equal to module size E_i . For each inner vertex d_i of tree corresponds the area u_i , which is formed by convolution subtree cuts, and has as its root vertex d_i .

Let's consider, that vertexes d_i and d_j are daughter vertex of d_k and the areas u_i и u_j - corresponding d_i and d_j - are determined lower limits of their size (x_i, y_i), (x_j, y_j). The binary convolution is a fusion of areas u_i and u_j , formation of u_k , dimensioning for u_k and new sizes for u_i and u_j . Let us introduce two infix operators H and V.

The record $u_k = u_i H u_j$, means, that areas u_i and u_j merge horizontally in one area u_k . If $u_k = u_i B u_j$, then the areas u_i and u_j merge vertically.

Designate that $\max(x_1, x_2)$ is maximum value of x_1 and x_2 .

At the confluence of the horizontal:

$$y_k = \max(b_i, b_j);$$

$$x_k = a_i + a_j;$$

y_i and y_j will have the size equal $\max(b_i, b_j)$.

At the confluence of the vertical:

$$y_k = b_i + b_j;$$

$$x_k = \max(a_i, a_j);$$

x_i and x_j will have the size $\max(a_i, a_j)$ [4].

For example:

The module dimensions $\langle 4, 2, 1, 3, 5, 9, 6, 7, 8 \rangle$ are fixed. The area dimensions in accordance with the consistent convolution, will be defined as follows:

$$1. u_8 = 7 H 8;$$

$$y_8 = b_7 + b_8;$$

$$x_8 = \max(a_7; a_8).$$

$$2. u_7 = 6 \vee u_8;$$

$$y_7 = \max(b_6; y_8);$$

$$x_7 = a_6 + x_8) \text{ and etc.}$$

The final plan of allocated modules is presented in figure 8.

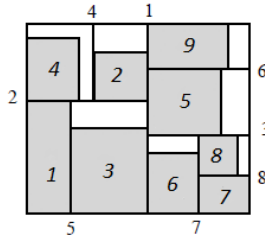


Fig. 8. The final plan of allocated modules

Step 6. Fitness function calculation.

Step 7. Selection. At each step of the evolution, individuals for next iteration are selected with the help of randomly selection operator. Selection allocates more copies of those solutions with higher fitness values and thus imposes the survival-of-the-fittest mechanism on the candidate solutions. The main idea of selection is to prefer better solutions to worse ones.

Step 8. The condition for the completion of the algorithm is the examination of the required number of iterations of the algorithm.

Step 9. Definition of the best individual (solution). The best solution of placement EC on PCB is the solution, which has the least result of fitness function.

Step 10. Result output.

IV. ACKNOWLEDGMENT

To confirm the efficiency of the algorithm for placement EC on PCB using the genetic algorithm of guillotine cutting method a special software was developed.

The study of the efficiency was carried out.

Investigation №1. Test launches of the program with constant initial data and the change in the number of generations of evolution were carried out.

The source and resulting data are presented in table 1.

TABLE I.

The number of the placement EC	The number of individuals in a population	The number of generations of evolution	f_c
50	10	10	666985
50	10	15	652074
50	10	20	587125
50	10	25	562158
50	10	30	478745
50	10	35	436585
50	10	40	395781
50	10	45	325641
50	10	50	284578
50	10	55	256485
50	10	60	256484
50	10	65	256484
50	10	70	256484

The table I is shown that with the increase of the generations of the evolution, the fitness-function decreases or remains unchanged, which testifies the optimal placement of the EC on the PP.

Investigation №2. Made a comparison of an iterative algorithm (IA) with our GA placement of EC on the PCB with the constant initial data.

TABLE II.

The number of the placement EC	f_{cGA}	f_{cIA}
10	5201	10257
20	82114	320458
30	157482	658921
40	304580	845225
50	478745	1036586
60	658148	1203558
70	851482	1698014
80	1201425	2003688
90	1582012	2365247
100	1965214	2875218

The table II is shown, that the values of the fitness-function GA is significantly less than the target function of iterative algorithm. Therefore, GA is more efficient than the standard algorithm.

V. CONCLUSION

In this paper proposed a developed software that implements automated procedures EC on PCB.

An important advantage of this software lies in the possibility taking into account the criteria of thermal conditions, while implementing the project the procedures, that will allow to increase the quality and reliability of the device.

The developed software integrates CAD-system Mentor Graphics Expedition PCB, which significantly increases the ease of use for end users.

In the future, the developed software product will be applied on a number of enterprises of Tatarstan for the design and development of printed circuit boards: "Радиоприбор", "Electronics", etc.

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